Radiation-Induced Fault Characterization in a 4-Bit D-Flip-Flop Shift Register Using LTSpice Transient Injection Analysis

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***Abstract*—This project investigates radiation-induced fault behavior in a 4-bit-serial-in/serial-out CMOS shift register constructed from transistor-level, transmission-gate D flip-flops in LTSpice. Transient current pulses emulating heavy-ion strikes are injected at all critical storage nodes, including Q, $\bar{Q}$, and internal master/slave latch nodes, to evaluate how charge deposition perturbs sequential state and propagates across pipeline stages. The analysis quantifies node-level susceptibility to Single-Event Upsets (SEU), Single-Event Transients (SET), and timing-related latch vulnerabilities. Sensitivity trends are correlated with electrical parameters such as node capacitance, drive strength, and logical/temporal masking. By mapping stage-by-stage vulnerability and identifying conditions under which disturbances persist or propagate, the study provides a structured methodology for SEE characterization in CMOS sequential circuits and informs the design of radiation-tolerant digital systems for space and aerospace applications.**

Keywords—radiation effects, single-event effects (SEE), single-event upset (SEU), single-event transient (SET), CMOS sequential logic, D flip-flop, shift register, transmission-gate flip-flop, transient current injection, LTSpice simulation, radiation tolerance, clock-phase sensitivity

When evaluating electronic systems for potential malfunction or degradation, radiation testing is essential, especially for circuits intended for high-altitude or space environments. High-energy particles such as heavy ions, protons, and neutrons can strike semiconductor material and deposit charges at sensitive regions. When this deposited charge is collected at a storage node in a CMOS (Complementary Metal-Oxide-Semiconductor) device, it can temporarily disturb the node voltage and corrupt the intended logic state [1][2][3][4]. CMOS logic, built from complementary PMOS and NMOS transistors, achieves low static power consumption, high switching performance, and broad applicability across microprocessors, memory, sensors, and embedded systems. Its widespread use makes understanding its radiation response a critical reliability concern.

Sequential logic is particularly susceptible to these disturbances. Unlike combinational circuits, which depend solely on present input values, sequential circuits store internal state that reflects both current and past inputs. This state, represented as a binary 0 or 1, is held in memory elements such as latches and flip-flops [4][5]. A radiation strike that deposits charge at a sensitive node can corrupt this stored value, causing a Single-Event Upset (SEU). Alternately, the strike may create a temporary voltage glitch known as a Single-Event Transient (SET), which may propagate through downstream logic. These Single-Event Effects (SEE) are especially concerning aerospace, satellite, avionics, and high-altitude systems, where reduced atmospheric density leads to higher exposure to energetic particles.

The circuit examined in this study is a four-stage D-flip-flop shift register. A shift register is a chain of flip-flops that stores and shifts data with each clock pulse, enabling applications such as serialization, configuration loading, counters, and communication interfaces [6]. The Serial-In Serial-Out (SISO) structure used in this work accepts data one bit at a time and shifts it through the system synchronously. Because each flip-flop stage depends on the previously stored value, the architecture behaves like a pipeline, meaning an upset introduced in one stage may propagate to subsequent stages. This makes a compact 4-bit shift register an effective test vehicle for studying SEE propagation, logical masking, temporal masking, and persistent multi-stage faults.

Many existing SEE studies focus on single flip-flops rather than multi-stage sequential pipelines. Additionally, much prior work uses behavioral-level modeling rather than full transistor-level CMOS representations. The present work addresses these limitations by implementing a complete transistor-level 4-bit CMOS transmission-gate D flip-flop shift register in LTSpice and performing node-accurate analysis across a realistic four-stage chain.

In this study, heavy-ion–equivalent transient current pulses are injected into all critical storage nodes, including Q, $\overline{Q}$, and the internal master and slave latch nodes of each flip-flop. The analysis quantifies node-level sensitivity to SEU, SET, and examines how these disturbances propagate or dissipate across multiple clock cycles. By correlating vulnerability with electrical parameters such as node capacitance, drive strength, and logical/temporal masking, the study identifies which stages and node types pose the greatest risk for persistent or propagating faults. This work establishes a structured and repeatable LTSpice methodology for SEE characterization in sequential logic and offers insights for designing radiation-tolerant digital systems for space-grade applications.

I. Radiation-Induced Single-Event Effects in CMOS Systems

A. Overview of Heavy-Ion Charge Deposition

When using heavy ions for electronic qualification testing, scientists examine how these particles lose energy as they travel through semiconductor material. As a heavy ion passes through silicon, it generates dense ionization along its trajectory, producing electron-hole pairs in what is often modeled as a cylindrical column of charge. The rate at which energy is deposited is quantified by the Linear Energy Transfer (LET), defined as the energy transferred per unit path length as an ionizing particle moves through a medium, typically expressed in kiloelectron-volts per micrometer (keV/μm) [7]. A high LET indicates that a heavy, highly charged particle deposits energy densely along a short path, which can produce severe localized charge deposition. Conversely, lower-LET radiation sources, such as x-rays, deposit energy more sparsely over longer or less-direct paths, causing less concentrated disturbance [7].

Charges created along the ion track may reach sensitive areas of a circuit through several physical mechanisms. Drift occurs when electric fields surrounding a junction pull carriers into sensitive nodes. Diffusion refers to the gradual spreading of carriers from regions outside the depletion region, allowing charge to reach nodes not directly in the strike path. Funneling describes a transient expansion of the depletion region following a strike, which effectively increases the volume from which charge can be collected. Together, these mechanisms determine how much of the ion-generated charge is ultimately collected at a node.

In CMOS circuits, sensitive nodes are typically the drain regions of transistors connected to storage elements such as latch nodes or Q/$\overline{Q}$ outputs. Low-capacitance nodes are particularly vulnerable because a given amount of collected charge produces a larger voltage perturbation compared to higher-capacitance nodes. If this perturbation exceeds the node's critical charge, the stored logic value may change, resulting in a transient disturbance or a data error such as a Single-Event Upset (SEU). Although low-capacitance nodes are essential for high-speed, high-frequency digital applications, enabling fast transitions, reduced power consumption, and improved signal integrity, they also carry an inherent tradeoff in susceptibility to radiation-induced charge collection [8].

B. Single-Event Upsets (SEU) in Storage Elements

A Single-Event Upset (SEU) occurs when an energetic particle passes through semiconductor material and generates a dense track of electron–hole pairs, producing a transient current pulse at a sensitive node. If the collected charge from this pulse exceeds the node's critical charge, the voltage at that node can be driven across the switching threshold of the storage element, resulting in a change of the stored value. In the context of this work, such an event may flip the logic state in one of the D flip-flops within the 4-bit shift register.

SEUs are typically classified as "soft" errors, meaning they do not permanently damage the device. Instead, the incorrect state persists only until the system overwrites it through normal operation, for example, on a subsequent clock cycle, refresh event, or reset. SEUs commonly affect memory structures such as SRAM or DRAM arrays, where storage nodes are small and highly sensitive to charge deposition. In sequential logic such as flip-flops, the bistable cross-coupled inverter structure amplifies the disturbance, enabling an upset to occur when the node voltage is briefly perturbed.

Cosmic rays and solar energetic particles (SEPs) are primary causes of SEUs in high-altitude and space environments, where reduced atmospheric shielding increases the likelihood of particle interactions. Importantly, SEUs can be more severe when strikes occur on internal latch nodes rather than on observable nodes such as Q, because internal nodes often have lower capacitance and weaker restoring drive strength. These behaviors and mechanisms are documented extensively in the radiation-effects literature [9][10].

C. Single-Event Transients (SET) and Signal Propagation

A Single-Event Transient (SET) occurs when charge deposited by an energetic particle briefly perturbs the voltage at a transistor node, producing a temporary pulse immediately flipping the stored state. When a high-energy particle such as a cosmic ray strikes a sensitive junction, it generates a dense cloud of electron-hole pairs. These carriers are rapidly separated by local electric fields, creating a transient current that momentarily alters the node voltage and forms a voltage glitch within the integrated circuit.

An SET pulse typically exhibits a fast rise followed by an exponential decay. The shape and duration of the pulse are determined by factors such as the node's resistance, capacitance, transistor drive strength, and the amount of collected charge. Although an SET does not inherently change the stored bit in a latch or flip-flop, it can interfere with downstream logic and produce more serious faults.

SETs become particularly problematic when the transient pulse is interpreted as a valid logic signal. If

the pulse propagates through combinational logic and arrives at a flip-flop input during a clock sampling window, it may be latched as data, effectively converting the SET into a Single-Event Upset (SEU). Because SETs can travel through multiple logic stages, a transient occurring early in a pipeline may influence later flip-flops depending on propagation delay and clock alignment. This makes SET behavior especially important in multi-stage sequential systems such as shift registers, where timing relationships dictate whether a transient is masked, attenuated, or captured.

II. 4-Bit Shift Register Architecture

The circuit explored within this report is a 4-bit D-flip-flop Shift Register Architecture. This section is going to explore this architecture in detail.

A. CMOS Transmission-Gate D Flip-Flop Design

Each stage of the shift registers in this circuit implemented using a transmission-gate based D flip-flop, a common CMOS topology that provides full-rail logic levels, low static power, and noise margins. The first step in creating a D flip-flop is to create a transmission gate, which consists of a parallel combination of PMOS and NMOS transistors whose source and drain terminals are tied together. When driven by complementary clock signals, the transmission gate behaves as a bidirectional switch that conducts strongly for both logic levels, avoiding the threshold-voltage degradation seen in single-transistor pass-gate designs [12] [13].

In a transmission-gate D flip-flop, these switches are used to form two level-sensitive latches, commonly referred to as the master and slave latches, connected in series. The master latch is enabled when the clock is low, allowing the input data (big voltage spike) to propagate to its internal storage node, while the slave latch holds its previous value. When the clock transitions high, the master latch becomes opaque and stores its captures value, while the slave latch becomes transparent and updates the output. This complementary clocking arrangement produces edge-triggered behavior, ensuring that the output changes only on the active clock edge [14].

The CMOS transmission-gate topology is widely used in digital VLSI because it provides strong drive capability, low leakage, and full-swing logic levels across process and voltage variations. However, the internal storage nodes within the master and slave latches typically exhibit low capacitance and relatively weak restoring currents, making them particularly sensitive to radiation-induced charge deposition. As a result, these nodes often represent the most vulnerable strike locations for single event upsets and transient disturbances in sequential logic circuits.

B. Master-Slave Latch Structure and Internal Nodes

A transmission gate D flip flop operates using a master-slave latch configuration, where two level-sensitive latches are clocked on oppositive phases to achieve edge-triggered behavior. The master latch is transparent when the clock is low, allowing the input to propagate to its internal storage node, while the slave latch holds its previous value. When the clock transitions high, the master latch becomes opaque and stores its captured value, and the slave latch becomes transparent, updating the output. This complementary clocking ensures that the output changes only on the active clock edge, preventing input glitches from propagating directly to the output [15].

Each latch contains a pair of cross-coupled CMOS inverters, forming a bistable storage element. These inverters create several critical internal nodes, including the master storage node, slave storage node, and complementary feedback nodes. Because these nodes typically have low capacitance and weak restoring drive, they are highly sensitive to radiation-induced charge deposition. Prior radiation-effects studies show that internal latch nodes are among the most vulnerable locations for Single-Event Upsets (SEUs), as even small perturbations can drive the node voltage across the switching threshold and invert the stored state [16], [17]. Understanding the electrical characteristics of these nodes is therefore essential for analyzing SEE susceptibility in sequential CMOS circuits.

C. Serial-In/Serial-Out (SISO) Pipeline Operation

The 4-bit shift register used in this study follows a Serial-In/Serial-Out (SISO) architecture, where data enters through a single input and propagates through four cascaded flip-flop stages. On each rising clock edge, the bit stored in stage i is transferred to stage i+1, forming a synchronous pipeline. After four clock cycles, the input bit emerges at the serial output, completing the shift operation. SISO shift registers are widely used in digital systems for serialization, delay elements, configuration loading, and communication interfaces [18].

This pipeline-like behavior makes SISO architecture particularly useful for studying fault propagation. A radiation-induced upset at an early stage may propagate through multiple downstream stages depending on logical masking, temporal masking, and the timing relationship between the transient and the clock edge. Prior work on multi-stage SEE propagation shows that sequential pipelines can amplify or extend the duration of Single-Event Transients (SETs), especially when the transient aligns with the sampling window of downstream flip-flops [19]. Thus, the SISO structure provides a compact and realistic platform for evaluating how SEEs evolve across multiple clock cycles.

D. Identification of Strike Locations (Q, $\bar{Q}$, Internal Nodes)

To evaluate radiation susceptibility across the entire shift register, transient current pulses were injected at all major storage and output nodes of each flip-flop stage. These include Q output node (which drives the next stage), $\bar{Q}$ complement node (part of the cross-coupled inverter pair), master latch internal storage node, slaves latch internal storage node.

These nodes represent the primary charge-collection sites in CMOS for sequential logic. Internal nodes typically have the smallest capacitances and weakest restoring currents, making them the most vulnerable to SEUs. In contrast, the Q and $\overline{Q}$ nodes often exhibit stronger electrical masking due to higher drive strength and fan-out loading, which can attenuate or suppress transient disturbances [16] [20].

By systematically injecting heavy-ion-equivalent current pulses at each node across all four stages, the analysis captures both local upset behavior and multi-stage propagation effects. This approach provides a comprehensive methodology for characterizing Single-Event Effects in sequential CMOS circuits and identifying the nodes most likely to produce persistent or propagating faults.

III. Methodology

The methodology used in this study established a structure and repeatable process for evaluating radiation-induced SEEs in a 4-bit CMOS transmission-gate D flip flop shift register. All simulations for testing were conducted in LTSpice implementing transistor-level models to ensure accurate representation of charge collection, node capacitances, and transient behavior. The procedure consists of four major components: circuit construction, baseline functional verification, transient current pulse injection, and multistage fault analysis.

A. Circuit Implementation in LTSpice for Simulation

A completed transitor-level schematic of a 4-bit Serial-In/Serial-Out shift register was implemented in LTSpice, and we can visualize one of the transmission gate master-slave D flip-flop as shown in Figure 1. Each stage consists of a CMOS transmission-gate-based master-slave D flip-flop constructed from complementary NMOS and PMOS devices. Level 1 MOSFET models were used for all transistors to ensure uniform electrical characteristics across all stages. The supply voltage was set to VDD = 5 V, matching the operating conditions used throughout the study.

A global clock signal (CLK) and its complement (CLK̄) where generated using voltage pulse sources and an inverter to provide non-overlapping control of master and slave lacthes. The Q output of each flip-flop was directly connected to the input of the subsequent stage, formung a four stage synchronous pipeline with a single serial input and serial output.

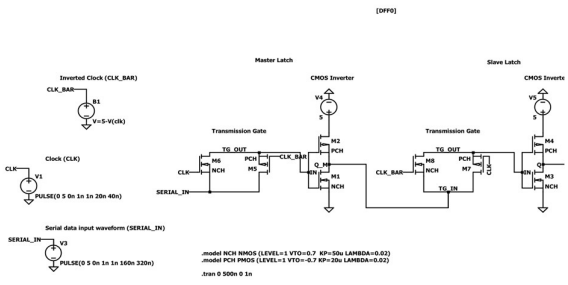

Fig. 1. Transistor-level schematic of one master–slave D flip-flop stage illustrating the structure used in each bit of the 4-bit serial-in/serial-out shift register.

B. Baseline Functional Verification

Before introducing radiation effects, baseline transient simulations were performed to verify correct logical operation of the shift register, A predefined SERIAL_IN waveform was applied, and transient analysis was run over multiple clock cycles. Internal latch nodes, Q/$\overline{Q}$ outputs, and the SERIAL_OUT node were monitored to confirm correct edge-triggered behavior, proper bit shifting, and full-rail logic levels. This step ensured that the circuit operated as intended prior to disturbance injection.

C. Radiation Strike Modeling Using Transient Current Injection

Radiation effects were modeled using transient current injection, a standard circuit-level technique for approximating heavy-ion charge deposition. A pulsed current source was connected to selected sensitive nodes, as illustrated in Fig. 2 (radiation strike injection configuration overlaid on the circuit schematic). The primary strike location used in this study was the master latch storage node (Q_M), identified as a representative low-capacitance storage node in transmission-gate-based flip-flops.

The injected current pulse was defined using a parameterized PULSE source with the following characteristics:

- Amplitude (I_strike): 2 mA
- Rise time: 50 ps
- Fall time: 50 ps
- Pulse width: 2 ns

This waveform approximates the fast transient current generated by charge collection following a heavy-ion strike. The strike timing relative to the clock (t_d) was treated as a swept parameter to evaluate sensitivity across different clock phases.

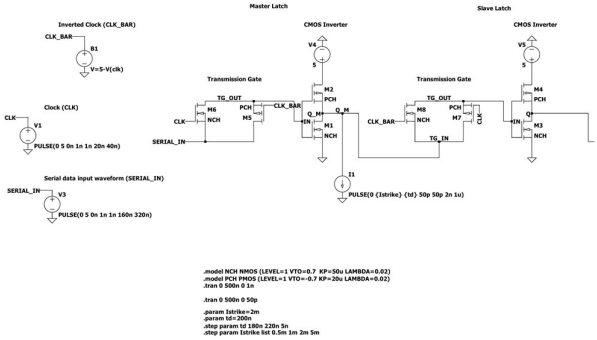

Fig 2. Transient current injection setup used to model radiation strikes, showing the pulsed current source connected to the master latch storage node (Q_m).

D. Timing Sweep and Clock-Phase Excitation

To capture the dependence of radiation response on clock phase, the strike timing parameter (t_d) was

swept from 180 ns to 220 ns in 5 ns increments using a stepped transient analysis. This sweep was chosen to span multiple regions of the clock cycle, including periods when the master latch is transparent, when the slave latch is transparent, and when both latches are isolated. By injecting identical current pulses at controlled time offsets, the methodology enabled direct comparison of circuit response as a function of strike timing.

E. Node Monitoring and Data Collection

During each simulation run, node voltages were recorded at the master latch storage node, internal transmission-gate nodes, Q/$\overline{Q}$ outputs, and the SERIAL_OUT node. Transient waveforms were captured over several clock cycles following each injection to allow observation of immediate disturbances as well as any subsequent state changes. This comprehensive node monitoring ensured that both localized effects and downstream behavior could be evaluated.

F. Multi-Stage Evaluation and Repeatability

All simulations were conducted using identical circuit parameters, clock conditions, and analysis windows to ensure repeatability. The same injection methodology was applied consistently across the shift register stages, allowing controlled comparison of node susceptibility and potential error propagation through the pipeline. This structured approach provides a repeatable framework for assessing radiation susceptibility in CMOS sequential logic and supports systematic evaluation of SEE mechanisms without reliance on behavioral-level abstractions.

IV. Results and Findings

A. Baseline Functional Operation

Before testing radiation effects, we first ran transient simulations to make sure that the circuit worked correctly by using the given SERIAL_IN waveform and complementary clock signals. The 4-bit serial-in/serial-out shift register showed us stable and repeatable behavior across multiple cycles. All the nodes, including the latch storage nodes, Q/ $\overline{Q}$ outputs, and SERIAL_OUT, switched very cleanly between the logic states and settled near the expected voltage levels, which were around 4.37 and 4.38 volts. The stable baseline behavior of internal latch nodes and SERIAL_OUT signal is shown in Fig. 3. On each rising clock edge, the stored value was properly transferred from one flip-flop stage to the next, which confirmed the edge-triggered operation of the transmission-gate master-slave D flip-flops. We ended up not seeing any glitches, metastability, or timing issues throughout the experiment. This made sure that any later disturbances during radiation injection were due to the injected charge and not due to the design errors.

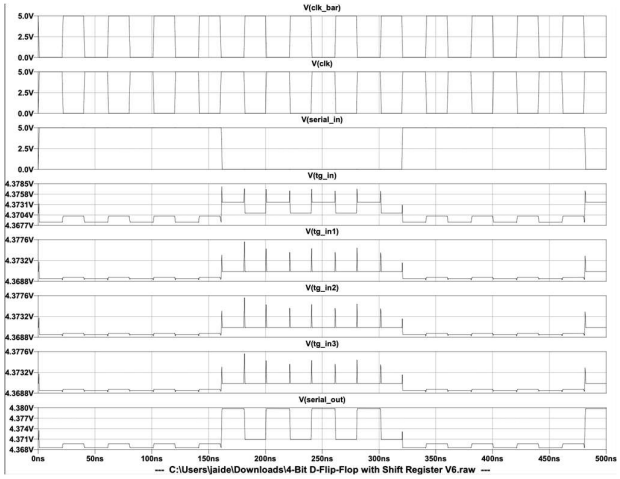

Fig. 3. The 4-bit shift register exhibits stable periodic operation under the applied CLK and SERIAL_IN stimuli. Node voltages settle to a consistent logic-high level (~4.37 V in this model) and maintain repeatable switching behavior over the simulated interval.

B. Response to Transient Current Injection at Master Latch Node

To study the radiation effects, we injected a transient current pulse at the master latch storage node (Q_m), which is essentially a sensitive, low-capacitance node. The pulse had a peak of about 2mA along with rise/fall times of 50ps, and a width of 2ns. This was meant to mimic charge collection from a heavy-ion strike. We varied the strike timing (t_d) from 180ns to 220ns in 5ns steps. From this sweep, we ended up seeing two main types of responses, which were Single-Event Transients and Single-Event Upsets. The one that showed up depended on how the strike lined up with the clock phase.

C. Single-Event Transient Behavior

When the strike occurred outside of the latch sampling window, we saw some short disturbances at many transmission-gate nodes, which were tg_in, tg_in1, tg_in2, and tg_in3. These appeared to look like narrow voltage spikes that were only tens of millivolts high and lasting a few nanoseconds. The Sing-Event Transients were strongest when the master latch was transparent or during clock transitions, due to the node of isolation being weaker. However, the spikes faded quickly and did not last beyond one cycle. The feedback from the cross-coupled inverters and the slave latch's isolation kept them from reaching the Q outputs or the SERIAL_OUT. This basically shows that the circuit masked these short disturbances unless the strike ended up happening right in the vulnerable timing window. Examples of these short-duration SETs at internal transmission-gate nodes following current injection at Q_m are shown in Fig. 4.

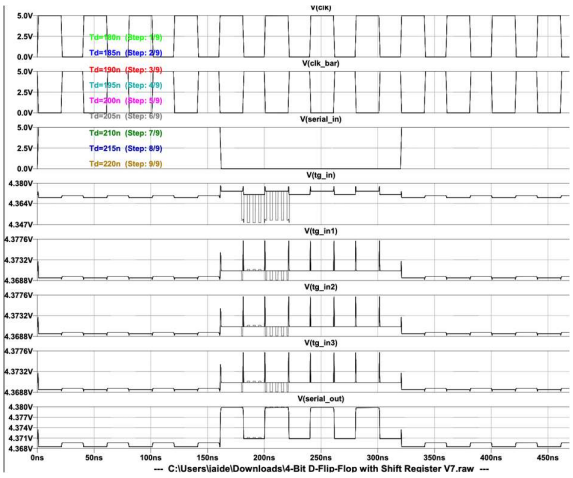

Fig. 4. A transient current pulse was applied as a radiation-strike proxy at the selected sensitive node using a parameterized PULSE source and a timing/charge sweep framework. The resulting node responses were evaluated for transient disturbances (SET) and persistent state inversions (SEU) using both direct node sampling and downstream observables.

D. Single-Event Upset Occurrence and Persistence

For certain timings, the disturbance ended up flipping the stored bit and staying flipped, which is considered a Single-Event Upset. This happened when the strike was between about 195ns and 205ns, with the worst case near t_d roughly about 200ns. This can be visualized in Fig. 5. That timing matches when the master latch is switching from transparent to opaque while the slave latch is closing, so the restoring strength ends up being weaker. In this situation, the injected charge happened to be enough to beat the latch's feedback, causing a permanent inversion of the stored value. The wrong bit then moved through the later flip-flop stages and showed up at SERIAL_OUT, proving that the Single-Event Transient was visible at the system level and not just local to the struck node.

td(ns)	Result
180-190	Mostly SETs, no permanent upset
195-205	**SEU Observed**
210-220	No upset (fully Masked)

Fig. 5. Exact vulnerable timing window. Worst case occurrs at roughly td = 200ns, which aligns with mater latch transparency, slave latch closing, and minimum restoring length.

E. Temporal Sensitivity and Clock-Phase Dependence

The timing sweep made it very clear that the circuit response depends heavily on the clock phase, due to striking before the active edge only causing the Single-Event Transients to be masked. Strikes that were right in the transparency window caused Single-Event Upsets, and strikes after the sampling window had no effect. The vulnerable window for Single-Event Upsets was about 10-15ns wide, showing that latch transparency and clock timing are the main factors for upset susceptibility. This matches what is expected from the temporal masking in sequential CMOS logic.

F. Propagation Through the Shift Register Pipeline

Once a Single-Event Transient occurred at the master's latch, the wrong bit kept moving through the register stage by stage with each clock cycle. SERIAL_OUT showed incorrect values for multiple cycles, which basically means that the shift register doesn't block errors and instead passes them along. This result shows that a single upset at an internal latch node can cause multi-cycle data corruption in a sequential pipeline, even without more strikes. It highlights that basic SISO shift registers don't have built-in fault containment.

V. Conclusion

The transient current injection experiments conducted in LTSpice through simulation on the 4-bit CMOS transmission-gate D flip-flop shift register showed clear and radiation induced behaviors that depended on node location and clock phase. Before any radiation effects were added, the shift register worked correctly, since all latch nodes and outputs switched accurately between logic high and logic low and shifted data properly on each rising clock edge, as shown in Fig. 3. This confirmed that any changes seen later were caused by the injected current and not by design errors.

When a 2 mA, 2 ns current pulse was injected at the master latch storage node, two distinct radiation effects were observed depending on the timing of the strike. When the strike occurred outside of the latch sampling window, small voltage spikes appeared at internal transmission-gate nodes (tg_in, tg_in1, tg_in2, and tg_in3). As visualized, these spikes were only tens of millivolts and lasted for just a few nanoseconds, which we can consider small spikes. As shown in Fig. 4, these Single-Event Transients were quickly suppressed and did not influence the Q outputs or the SERIAL_OUT signal. This shows that the circuit was able to mask these short disturbances when the strike timing was not critical.

In contrast, when the current pulse was injected during a narrow timing window while the latch was changing state, a Single-Event Upset was observed. Strikes between about 195 ns and 205 ns caused the stored value at the master latch to flip and stay flipped. The most significant case was observed near 200 ns, as shown in Fig. 5. At this time, the master latch was closing while the slave latch was also closing, which made the latch weaker and easier to upset. The vulnerable window was about 10–15 ns wide, showing that the circuit is very sensitive to clock timing, and shows heavy dependency on the clock phase.

Once an SEU occurred, the wrong bit moved through the shift register with each clock cycle, which led to inaccurate outputs. The incorrect value appeared at the SERIAL_OUT node for multiple cycles, showing that the error was not fixed on its own. The results showcased in section V help us visualize how even a single upset at an internal latch node can result in a

multi-cycle output inaccuracy in a simple serial-in/serial-out shift register.

Overall, the simulation results demonstrated that transmission-gate D flip-flops are most vulnerable to radiation strikes at internal latch nodes, especially when the strike happens during a critical clock window. While many short transients are masked, strikes during this window can cause permanent bit flips that spread through the system. This shows that basic shift-register designs do not protect against radiation-induced errors and need additional protection when used in radiation-exposed environments.

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